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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,961	07/30/2003	Robert A. Corley	1-1	1792

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EXAMINER	
DAVENPORT, MON CHERI S	

ART UNIT	PAPER NUMBER
2416	

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11/25/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/630,961	CORLEY ET AL.	
	Examiner	Art Unit	
	MON CHERI S. DAVENPORT	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/2/2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. In view of the Appeal brief filed on 9/2/2008, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

/Seema S. Rao/

Supervisory Patent Examiner, Art Unit 2416.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1-14** rejected under 35 U.S.C. 103(a) as being unpatentable over Mazzola (US Patent Number 5,278,834) in view of Hamacher et al. (Computer Organization, 1984) .

Regarding **claim 1** Mazzola discloses a processor comprising (see figure 1):

controller circuitry configurable to determine for a given protocol data unit received by the processor(figure , section 12, processor) whether the given protocol data unit is a single-cell protocol data unit***(see figure 1, section 10, end-system processing node, see col. 7, lines 29-34, the size of the data is compared to a predetermined maximum size limit of envelope field to determine whether once the protocol layer headers are added , the result PDU would be too large to send out from the source nodes a single data unit);*** and

the processor being connectable to second memory circuitry external to the processor***(see col 3, lines 42-47, stack manager is a second internal used memory, third area 14c, (reads on second memory externally, note that is located in a different area external to the processor (section 12)) of memory is the buffer pool from which message buffer are allocated)*** ;

wherein information characterizing the given protocol data unit is stored in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit ***(see col 3-4, lines 58-25, stack 14a, permits data to be passed vertically between protocol layers, the memory buffer, stores the protocol control information which is added in the form of a header, the buffer contains a PDU big enough to be transmitted as single data unit, see also col. 2, lines 25-30,col. 2 lines 52-55, a portion of the buffer contains a least a portion of the message, and is sufficiently small that it may contain a(single-cell) PDU to be sent out from the lowest layer of the protocol stack)***

wherein information characterizing the given protocol data unit is stored in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit ***(see col. 4,***

lines 11-20, a block message that is too large to be transmitted as a single block of data is pre-segmented and a layer header is added).

Mazzola fails to specifically point out that the first memory is internal to the processor as claimed.

However Hamacher et al. teaches the first memory is internal to the processor (see pg. 6, section Arithmetic and logic unit, paragraph 2, lines 3-8, processors contain high speed storage(memory) call registers for temporary storage)

Therefore it would have been obvious to combine Mazzola's invention with Hamacher et al. because internal registers (memory) is 5-10 times faster than external memory to process single-cell PDU's from internal memory. Because doing so would gain a 5-10 times speedup in processing those single-cell PDU's.

Regarding **Claim 2** Mazzola discloses everything as applied above (*see claim 1*). In addition the processor includes:

wherein the protocol data unit comprises a packet ***(see col. 3, lines 33-35, the invention can be used with any packet based being that data is formatted into PDU's)***

Regarding **Claim 3** Mazzola discloses everything as applied above (*see claim 1*). In addition the processor includes:

wherein the single-cell protocol data unit comprises a protocol data unit having a size less than or substantially equal to that of a cell-based processing unit of a switch fabric associated with the processor ***(see figure 1, section 10, end-system processing node, see col. 7, lines 29-34,***

the size of the data is compared to a predetermined maximum size limit of envelope field to determine whether once the protocol layer headers are added , the result PDU would be too large to send out from the source nodes a single data unit).

Regarding **Claim 4** Mazzola discloses everything as applied above (*see claim 1*). In addition the processor includes:

wherein the information characterizing the given protocol data unit comprises at least one block descriptor ***(see col. 4, lines 8-11, the buffer contains at least part of the message data as well as headers from the protocol layers of the source stack).***

Regarding **Claim 5** Mazzola discloses everything as applied above (*see claim 1*). In addition the processor includes:

wherein the block descriptor ***(header)*** is associated with a particular data block of the given protocol data unit***(see col. 4, lines 15-20, the PDU is segmented and a header is added).***

Regarding **Claim 6** Mazzola discloses everything as applied above (*see claim 1*). In addition the processor includes:

wherein the information characterizing the given protocol data unit is stored in the first memory circuitry without requiring utilization of a linked list data structure ***(see col. 7, lines 29-34, the size of the data is compared to a predetermined maximum size limit of envelope field to determine whether once the protocol layer headers are added , the result PDU would be too large to send out from the source nodes a single data unit)***.

Regarding **Claim 7** Mazzola discloses everything as applied above (*see claim 1*). In addition the processor includes:

wherein the information characterizing the given protocol data unit is stored in the second memory circuitry utilizing a linked list data structure ***(see col. 7, lines 34-46, buffers are chained as linked list) .***

Regarding **Claim 8** Mazzola discloses everything as applied above (*see claim 1*). In addition the processor includes:

wherein the processor is configured to provide an interface for communication of the protocol data unit between a network and a switch fabric ***(see figure 1, section 15, network interface).***

Regarding **Claim 9** Mazzola discloses everything as applied above (*see claim 1*). In addition the processor includes:

wherein at least one of the first memory circuitry and the second memory circuitry further comprises a queuing and dispatch buffer memory of the processor ***(see figure 1, section 14b, stack manager, see col 3. , lines 42-45).***

Regarding **Claim 10** Mazzola discloses everything as applied above (*see claim 1*). In addition the processor includes:

wherein at least one of the first memory circuitry and the second memory circuitry further comprises a PDU buffer memory of the processor ***(see figure 1, section 14c, buffer pool, see col. 3, lines 45-48).***

Regarding **Claim 11** Mazzola discloses everything as applied above (*see claim 1*). In addition the processor includes:

wherein the processor comprises a network processor ***(see figure 1, section 12, processor).***

Regarding **Claim 12** Mazzola discloses everything as applied above (*see claim 1*). In addition the processor includes:

wherein the processor is configured as an integrated circuit ***(see col. 3, lines 19-26)***

Regarding **Claim 13** Mazzola discloses a method for use in a processor comprising controller circuitry and first memory circuitry internal to the processor, the processor being connectable to second memory circuitry external to the processor, the method comprising the steps of (see figure 1):

determining for a given protocol data unit received by the processor whether the given protocol data unit is a single-cell protocol data unit (***see col. 7, lines 29-34, the size of the data is compared to a predetermined maximum size limit of envelope field to determine whether once the protocol layer headers are added, the result PDU would be too large to send out from the source nodes a single data unit)***;

storing information characterizing the given protocol data unit in the first memory circuitry (see figure 1, section 14a and 14b) if the given protocol data unit is a single-cell protocol data unit ***(see col 3-4, lines 58-25, the memory buffer, stores the protocol control information which is added in the form of a header, the buffer contains a PDU big enough to***

be transmitted as single data unit, see also col. 2, lines 25-30,col. 2 lines 52-55, a portion of the buffer contains a least a portion of the message, and is sufficiently small that it may contain a(single-cell) PDU to be sent out from the lowest layer of the protocol stack); and

storing information characterizing the given protocol data unit in the second memory circuitry (see figure 1, section 14c, buffer pool) if the given protocol data unit is not a single-cell protocol data unit ***(see col. 4, lines 11-20, a block message that is too large to be transmitted as a single block of data is pre-segmented and a layer header is added)***

Mazzola fails to specifically point out that the first memory is internal to the processor as claimed.

However Hamacher et al. teaches the first memory is internal to the processor (see pg. 6, section Arithmetic and logic unit, paragraph 2, lines 3-8, processors contain high speed storage(memory) call registers for temporary storage)

Therefore it would have been obvious to combine Mazzola's invention with Hamacher et al. because internal registers (memory) is 5-10 times faster than external memory to process single-cell PDU's from internal memory. Because doing so would gain a 5-10 times speedup in processing those single-cell PDU's.

Regarding **Claim 14** Mazzola discloses a processor-readable medium containing processor-executable instructions for use in a processor comprising controller circuitry and first memory circuitry internal to the processor, the processor being connectable to second memory circuitry external to the processor, the instructions when executed in the processor implementing the steps of:

determining for a given protocol data unit received by the processor whether the given protocol data unit is a single-cell protocol data unit (***see col. 7, lines 29-34, the size of the data is compared to a predetermined maximum size limit of envelope field to determine whether once the protocol layer headers are added, the result PDU would be too large to send out from the source nodes a single data unit)***;

storing information characterizing the given protocol data unit in the first memory circuitry (see figure 1, section 14a and 14b) if the given protocol data unit is a single-cell protocol data unit ***(see col 3-4, lines 58-25, the memory buffer, stores the protocol control information which is added in the form of a header, the buffer contains a PDU big enough to be transmitted as single data unit, see also col. 2, lines 25-30,col. 2 lines 52-55, a portion of the buffer contains a least a portion of the message, and is sufficiently small that it may contain a(single-cell) PDU to be sent out from the lowest layer of the protocol stack)***; and

storing information characterizing the given protocol data unit in the second memory circuitry (see figure 1, section 14c, buffer pool) if the given protocol data unit is not a single-cell protocol data unit ***(see col. 4, lines 11-20, a block message that is too large to be transmitted as a single block of data is pre-segmented and a layer header is added)***.

Mazzola fails to specifically point out that the first memory is internal to the processor as claimed.

However Hamacher et al. teaches the first memory is internal to the processor (see pg. 6, section Arithmetic and logic unit, paragraph 2, lines 3-8, processors contain high speed storage(memory) call registers for temporary storage)

Therefore it would have been obvious to combine Mazzola's invention with Hamacher et al. because internal registers (memory) is 5-10 times faster than external memory to process single-cell PDU's from internal memory. Because doing so would gain a 5-10 times speedup in processing those single-cell PDU's.

Response to Arguments

3. Applicant's arguments with respect to claims 1, 13, and 14 have been considered but are moot in view of the new ground(s) of rejection.

In the remarks on pg. 5 of the appeal brief, the applicant contends that Mazzola does not teach or suggest "wherein information characterizing a given protocol data unit is stored in the first memory circuitry if the given protocol data unit is a single cell protocol data unit, and information characterizing the given protocol data unit is stored in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit"

Examiner respectfully disagrees Mazzola teaches that a single-cell PDU is stored in a single (first) memory buffer which reads on the claim language of first memory circuitry. Multiple-cell PDUs are stored in a link list (second memory circuitry) if not a single cell PDU.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MON CHERI S. DAVENPORT whose telephone number is (571)270-1803. The examiner can normally be reached on Monday - Friday 8:00 a.m. - 5:00 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Seema S. Rao/
Supervisory Patent Examiner, Art Unit 2416

/Mon Cheri S Davenport/
Examiner, Art Unit 2416
November 21, 2008